REMARKS

I. Formalities

Applicant thanks the Examiner for considering the references cited with the Information Disclosure Statement filed on May 16, 2006.

II. Status of the Application

By the present amendment, Applicant amends claims 29-31 and 33. Claims 13-14, 16 and 29-34 are all the claims pending in the Application, with claim 29 being in independent form. Claims 13-14, 16 and 29-34 have been rejected.

The present amendment addresses each point of objection and rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

III. Claim Rejections Under 35 U.S.C. § 103

A. Independent Claim 29

The Examiner has rejected claims 16, 29 and 33-34 under 35 U.S.C. §103(a) as allegedly being unpatentable over the Prior Art as admitted by Applicant, in view of U.S. Patent Publication No. 2003/0025127 A1 to Yanai et al. (hereinafter "Yanai") and Japanese Patent Application No. 2003-017502A to Nakamura (hereinafter "Nakamura"). Applicant respectfully traverses these rejections for *at least* the reasons set forth below.

The Examiner previously indicated that claim 29 was allowable because the prior art neither taught nor suggested the feature of "wherein said third gate electrode has the same thickness as said first gate electrode," as claimed. However, in the outstanding Office Action, the Examiner now cites the Nakamura reference as allegedly teaching or suggesting this feature.

In particular, the grounds of rejection allege that the gate electrode 13, as taught in Nakamura, is similar in its requirements to the recited first transistor with source/drain regions formed in a self-aligning manner. As such, the grounds of rejection allege that because of the similar functional requirements between Nakamura's gate electrode 13 and the recited first electrode, it would have been obvious to one of ordinary skill in the art to apply the same physical dimensions to both of these electrodes. Further, the grounds of rejection allege that the requirement of equal thickness is essentially a range limitation of a thickness difference being zero and that the present specification does not teach why the third gate electrode having the same thickness as the first gate electrode is critical to the claimed invention.

Applicant respectfully disagrees with the grounds of rejection. In order for the Examiner to maintain a rejection under 35 U.S.C. §103, Yanai, Nakamura, or some combination thereof, must teach or suggest all of the recitations of claim 29. Applicant respectfully submits that, even if one of ordinary skill in the art were to combine the teachings of Yanai and Nakamura as proposed in the grounds of rejection, such a proposed combination nevertheless fails to teach or suggest all of the recitations of claim 29.

Independent claim 29 has been amended to recite (among other things):

> ...a low voltage driving thin film transistor formed above said insulating substrate, wherein said low voltage driving thin film transistor comprises... a first gate insulating film formed on said first active layer...
>
> wherein said high voltage driving thin film transistor further comprises a third gate electrode driven at low voltage... wherein said third gate electrode is formed between said second active layer

and said second gate electrode and on the first gate insulating film...

Without conceding the merits of the Examiner's rejections, Applicant has amended claim 29, as set forth above, to require that the first gate electrode and the third gate electrode are formed on a same layer (i.e., the recited first gate insulating film). This feature, among other things, reduces the processing steps for the thin film transistor substrate.

However, even if one of ordinary skill in the art were to apply the teachings of Nakamura to Applicant's Admitted Prior art, as shown in Figure 1, one still would not arrive at the invention claimed in claim 29. Contrary to the requirements of claim 29, Nakamura teaches a thin film transistor having gate electrode 13 and gate electrode 17, which is electronically connected to gate electrode 13 and is formed above gate electrode 13. (Figure 4A).

Therefore, if a skilled artisan were to apply the teachings of Nakamura to Applicant's Admitted Prior art, as shown in Figure 1, then the electrode 17 would be formed over gate electrode 304 and 307 because the electrode 17 is formed over main-gate electrode 13. Accordingly, the recitations of claim 29 would not have been obvious to one of ordinary skill in the art in view of the cited references for *at least* these reasons.

In further contrast to the recitations of claim 29, Figure 4A of Nakamura shows that the electrode 17 affects to the lightly doped drain region P:4E17/cm^3, and not to the channel region B:2E16/cm^3. (Figure 4A). Therefore, as taught in Nakamura, the electrode 17 cannot solely control the thin film transistor disclosed therein. In contrast, the third gate electrode (low voltage gate) 110 according to an exemplary embodiment of the present invention is facing to the second channel region 203 in the second active layer 102 so that the third gate electrode can solely

control the thin film transistor. (*See e.g.,* Figure 8). Furthermore, the second gate electrode (high voltage gate) 107 according to an exemplary embodiment of the present invention is also facing to the second channel region 203. As such, both the third gate electrode 110 and the second gate electrode 107 can independently control the on/off of the second channel region 203.

According to exemplary embodiments of the present invention, such a sub-gate structure is excellent in output controllability at a low gate voltage and, therefore, is appropriate for a high withstand voltage thin film transistor used for a level shift circuit. In other words, if an applied voltage to the high voltage driving thin film transistor is sufficiently lower than the predetermined operating voltage, then the applied voltage is shifted to the third gate electrode instead of the second gate electrode so that the current value increases. (*See* broken line in Figure 6). As a result, according to exemplary embodiments of the present invention, the on/off ratio of current value increases and output controllability is improved.

Indeed, as described in detail in the present specification, in the case where a circuit is formed by mixedly providing thin film transistors that adopt plural kinds of driving voltages, it is advantageous for lower power consumption of the circuit that main parts corresponding to a logic circuit, a shift register, and the like, are structured by low voltage driving thin film transistors. (*See e.g.,* paragraph 02). Therefore, it is better to avoid a parasitic capacitance in the low voltage driving thin film transistors, and the parasitic capacitance does not present a large problem depending on a circuit design in the high voltage driving thin film transistor.

In view of the above, Applicant respectfully submits that claim 29 would not have been obvious in view of Yanai, Nakamura, and any combination thereof, for *at least* these reasons.

Further, Applicant submits that claims 30-31 and 33 are patentable over the cited references *at least* by virtue of their dependency.

B. Independent Claim 30

The Examiner has also rejected claim 30 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art in view of U.S. Patent No. 5,053,849 to Izawa *et al.* (hereinafter "Izawa") and further in view of Nakamura.

Applicant has amended claim 30, as set forth above, to depend from claim 29. Applicant submits that claim 29 is patentable over the cited references for *at least* the reasons already discussed above. Further, Applicant submits that claim 30 is patentable over the cited references *at least* by virtue of its dependency. Thus, Applicant respectfully requests that the Examiner withdraw this rejection.

C. Independent Claim 31

The Examiner has rejected claim 31 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art in view of U.S. Patent No. 6,048,795 to Numasawa et al. (hereinafter "Numasawa") and further in view of Nakamura.

Applicant has amended claim 31, as set forth above, to depend from claim 29. Applicant submits that claim 29 is patentable over the cited references for *at least* the reasons already discussed above. Further, Applicant submits that claim 31 is patentable over the cited references *at least* by virtue of its dependency.

Thus, Applicant respectfully requests that the Examiner withdraw this rejection.

D. Dependent Claims 32

Finally, the Examiner has rejected claim 32, under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art, in view of Yanai, and further in view of Nakamura. The Examiner has rejected claim 13 as allegedly being unpatentable over Applicant's Admitted Prior Art, in view of Yanai, further in view of Nakamura, and further in view of U.S. Patent No. 5,757,050 to Adler (hereinafter "Adler"). The Examiner has rejected claim 14 as allegedly being unpatentable over Applicant's Admitted Prior Art, in view of Yanai, further in view of Nakamura, and further in view of U.S. Patent No. 6,507,069 to Zhang et al. (hereinafter "Zhang").

Claims 32, 13 and 14 all depend from claim 29. Applicant submits that claim 29 is patentable over the cited references for *at least* the reasons already discussed above. Therefore, Applicant submits that claims 32, 13 and 14 are patentable over the cited references *at least* by virtue of their dependency.

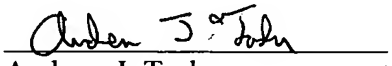
Hence, Applicant respectfully requests that the Examiner withdraw these rejections.

IV. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Andrew J. Taska
Registration No. 54,666

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: December 15, 2006